This listing of claims replaces all prior versions and listings of the claims in the application.

IN THE CLAIMS:

List of Pending Claims:

1. (Withdrawn) A hot-switchable voltage bus for IDDQ measurement, comprising:

a global voltage bus;

a quiescent voltage bus, separate from the global voltage bus;
at least one voltage island (Vi, V2, ….,Vn);

a system for selectively connecting each voltage island to the quiescent and

global voltage busses during IDDQ testing.

2. (Withdrawn) The hot-switchable voltage bus of claim 1, wherein the system for selectively connecting is configured to hot-switch each voltage island between the quiescent and global voltage busses.

3. (Withdrawn) The hot-switchable voltage bus of claim 2, wherein each voltage island does not lose state during the hot-switching between the quiescent and global voltage busses.

4. (Withdrawn) The hot-switchable voltage bus of claim 2, further comprising a global power supply for supplying a voltage VDDg to the global voltage bus and a quiescent power supply for supplying a voltage VDDq to the quiescent voltage bus.

5. (Withdrawn) The hot-switchable voltage bus of claim 4, wherein VDDg is equal to VDDq.

6. (Withdrawn) The hot-switchable voltage bus of claim 5, wherein the IDDQ measurement is performed independently for VDDg and VDDq.

7. (Withdrawn) The hot-switchable voltage bus of claim 1, wherein the system for selectively connecting comprises a header device (Hi, H2 Hn; Hiq, H2q Hnq)for selectively connecting each voltage island to the quiescent and global voltage busses in response to a control signal.

8. (Withdrawn) The hot-switchable voltage bus of claim I, further comprising a plurality of voltage sensors.

9. (Currently amended) A method [[for]] of performing a quiescent current (IDDQ) test~~ing~~ of a chip having V-islands coupled to control logic, the method comprising:

powering the chip through at least one global voltage bus and setting the chip in a quiescent state;

hot-switching at least one of the voltage islands (Vi, V2, ..., Vn) between a global voltage bus and a quiescent voltage bus; and

~~performing~~ measuring the IDDQ ~~testing~~ on the at least one voltage island.

10. (Currently amended) The method of claim 9, wherein each of the at least one voltage islands does not lose state during the hot-switching between the quiescent and global voltage busses.

11. (Original) The method of claim 9, further comprising:

supplying a voltage VDDg to the global voltage bus; and

supplying a voltage VDDq to the quiescent voltage bus.

12. (Original) The method of claim 11, wherein VDDg is equal to VDDq.

13. (Currently amended) The method of claim 9, wherein hot-switching further comprises:

providing a connection (H1, H2, ..., Hn; H1q, H2q, ..., Hnq) between each of the at least one voltage islands and the global and quiescent voltage busses; and

selecting at least one of the connections to connect each of the at least one voltage islands to at least one of the global and quiescent voltage busses.

14. (Original) The method of claim 13, wherein each connection includes a header device (H1, ….., H2, ..., Hn; H1q, H2q, …..,Hnq), and wherein each connection is selected by activating the header device of the connection via a control signal.

15. (Currently amended) The method of claim 9, wherein performing IDDQ testing comprises:

applying a test pattern to each of the at least one voltage islands, wherein the test pattern remains valid during hot-switching between the global and quiescent voltage busses.

16. (Original) The method of claim 9, further comprising:

hot-switching different sets of voltage islands between the global and quiescent voltage busses.

17. (Original) The method of claim 9, further comprising:

locating IDDQ defects using a resistance of the quiescent voltage bus.

18. (Original) The method of claim 9, wherein IDDQ testing is performed on individual voltage islands or sets of voltage islands.

19. (Original) The method of claim 9, further comprising:

obtaining IDDQ measurements from individual voltage islands or sets of voltage islands during the IDDQ testing; and

comparing the obtained IDDQ measurements to other IDDQ measurements.

20. (Original) The method of claim 19, wherein the obtained IDDQ measurements are compared to IDDQ measurements for similar circuitry, or wherein the obtained IDDQ measurements are compared to an average IDDQ measurement.

21. (Currently amended) A method comprising:

powering a chip having V-islands coupled to control logic at least one global voltage bus and setting the chip in a quiescent state;

hot-switching at least one voltage islands (V1, V2, ….,Vn) between a plurality of different voltage busses, wherein each voltage island does not lose state during the hot-switching; and

measuring a quiescent current ~~performing~~ (IDDQ) ~~testing~~ on the at least one voltage island.

22. (Currently amended) The method of claim 21, wherein each of the voltage buses provides a same voltage.

23. (Original) The method of claim 21, further comprising:

locating IDDQ defects in the at least one voltage island.

24. (Original) The method of claim 21, wherein the voltage busses comprise power supply busses or ground busses.

25. (Currently amended) A method for monitoring power consumption, comprising:

powering a chip having V-islands coupled to control logic at least one global voltage bus and setting the chip in a quiescent state;

connecting at least one voltage island (V1, V2, ….,Vn) to a quiescent voltage bus; and

monitoring power usage at a VDDq power supply connected to the quiescent voltage bus for the at least one voltage island.